IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#14
11/30/01
V. Vannal

Applicants:	Hsiao, Tommy C.; Hui, Angela T.; Ogle, Robert B.; Pham, Tuan Duc; Plat, Marina V.; Ramsbey, Mark T.; Shen, Lewis		
Assignee:	Advanced Micro Devices, Inc.		
Title:	Polished Flash Process With Metal Gates And Improved Planarity		
Serial No.:	09/430,366	Filing Date:	October 28, 1999
Examiner:	J. Chen	Group Art Unit:	2813
Docket No.:	M-7523 US		

San Jose, California
November 13, 2001

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

SUMMARY OF TELEPHONIC INTERVIEW WITH EXAMINER

Dear Sir:

The submission summarizes a telephonic interview between Examiner Jack Chen and Applicants' Attorney, F. Jason Far-hadian, on October 3, 2001, regarding the Office Action of August 15, 2001.

During the telephonic interview, Applicants' attorney noted that the cited portions of the reference (Mitchell et. al., Pat. No. 4,713,142) in FIGS. 2c-2e teach an insulator layer 37 formed over an oxide layer 36 and proposed amending the claims to recite "depositing an insulator layer of high temperature oxide *directly* over the substrate and the floating gate" to distinguish the invention over the cited reference. The Examiner agreed that depositing a single layer of high temperature oxide directly over the floating gate was not illustrated by the cited Figures. The Examiner, however, referred to language recited in Claim 1 of the cited reference (column 4, lines 53-55) that discloses "depositing a conformal layer of insulating material on the surface of said substrate and said conductive strips" (this language is neither cited nor relied upon in the Office Action of August 15, 2001). The Examiner contended that this language teaches forming an insulator layer directly over the

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

floating gate. The Applicants' Attorney responded that the additional elements claimed by the Applicants, such as "an insulator layer of high temperature oxide," are not taught or suggested by said language.

Examiner Chen, in the telephonic interview of August 3, 2001 also agreed with the Applicants' Attorney that "high temperature oxide" is known in the art. The Examiner indicated that he needs to further consider whether a "high-temperature oxide" is distinguishable over oxidation methods suggested by the cited reference. The Applicants' Attorney referred the Examiner to references cited in the Response to the Office Action of April 6, 2001 that indicate high temperature oxides are often formed by an LPCVD process.[1] All cited references fail to disclose a high temperature oxide.

The Examiner indicated that he would consider the arguments presented by the Applicants' Attorney in a written response and that he will call the Applicants' Attorney prior to issuing the next office action to discuss any allowable subject matter. Pursuant to the Examiner's request, Applicants will file a written Response to the Office Action of August 15, 2001.

EXPRESS MAIL LABEL NO.
EL901564881US

Respectfully submitted,

Edward C. Kwok
Attorney for Applicants
Reg. No. 33,938

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

[1] S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era, Vol. 1 - Process Technology p. 169, 184 (Lattice Press, 1986); Buried-Channel PMOSFET Elevated Source/Drain Using Self-Aligned Epitaxial Silicon Silver, Abstract, Senior Semiconductor Society, currently accessible at http://www.semicontech.com/korean/se2/se2-1a02.html.